

A NOVEL RESONANT-TYPE GaAs SPDT SWITCH IC WITH LOW DISTORTION CHARACTERISTICS FOR 1.9 GHz PERSONAL HANDY-PHONE SYSTEM

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ABSTRACT

A GaAs SPDT switch IC operating at a low power supply voltage of 2.7 V has been developed for use in Personal Handy-Phone System in the 1.9 GHz band. In combination with MESFETs with low on-resistance and high breakdown voltage, the resonant-type switch IC utilizes stacked FETs and an additional shunt capacitor at the receiver side in order to realize low insertion loss, high isolation and low distortion characteristics. An insertion loss of 0.55 dB and an isolation of 35.8 dB were obtained at 1.9 GHz. The IC also achieved a second order distortion of -54.3 dBc and an adjacent channel leakage power of -66 dBc at 600 kHz apart from 1.9 GHz at 19 dBm output power.

INTRODUCTION

The field of mobile communication has expanded to include L-band digital mobile radio systems such as the Japanese Personal Handy-Phone System (PHS). According to Ref [1], a $\pi/4$ -shifted QPSK output signal from PHS set needs to satisfy low distortion characteristics such as a high order distortion of less than -45 dBc and an adjacent channel leakage power of less than -50 dBc at 19 dBm output power in the transmitting mode. Thus, a Single Pole Double Throw (SPDT) switch IC needs to fulfill low distortion characteristics as well as low insertion loss and high isolation. However, it seems difficult to satisfy the requirements, especially the high order distortion below -45 dBc, using conventional switches with a low power supply voltage of 2.7 V. One method to overcome the problem is just to insert a filter between the switch and the antenna, although it leads to increase the total insertion loss from the output node of the power amplifier (PA), and thus to increase the total dissipated current for the PA. Another method is to apply positive/negative voltages to the control gates of FETs which leads to keep the off-state FET off [2]. However, in this case, it is necessary to generate negative voltage, which results in increasing the size and the dissipated currents in the system. This paper describes a novel SPDT switch IC with low insertion loss, high isolation

and low distortion characteristics so as to overcome the problem indicated above.

CIRCUIT DESIGN

In a conventional SPDT switch IC shown in Fig 1(a), shunt FETs are inserted for obtaining high isolation [3] [4]. However, transmitted RF signal leaks into the receiver side through source-drain stray capacitance of the off-state FET (C_{off}), and it also leaks into the ground-line through C_{off} at the transmitter side. The conventional switch requires large-size FETs with low on-resistance (R_{on}) for low insertion loss, while it is preferable to have small-size FETs so as to obtain high isolation. Thus, there is a trade-off between insertion loss and isolation for designing the conventional SPDT switches, or we have to develop high performance FETs which satisfy both low R_{on} and low C_{off} , which seems to be very difficult to realize.

Fig 1 (b) shows another switch configuration that has the inductors connected in parallel with the series FETs. Since the inductor and the stray capacitance of off-state FET (C_{off}) act as the parallel-LC resonator at 1.9 GHz, this switch features high isolation. By using this configuration, we can design the switch IC without considering the trade-off between insertion loss and isolation. In addition, it enables us to eliminate the shunt FETs which is used to obtain high isolation. However, these switches which are composed of only one series FET have poor distortion characteristics in the transmitting mode. With increasing the input RF power, larger RF signal voltage is applied to the output node of the series FET at the receiver side, and then the off-state FET finally turns on. To overcome this problem, we have proposed new switch IC configuration shown in Fig 1(c).

Fig. 1 (c) shows new resonant-type switch IC composed of three FETs, two inductors, five resistors and a shunt capacitor (C_X). At the receiver side, an FET and a parallel-LC resonator composed of an FET and an inductor are stacked in order to distribute an RF signal voltage swing, because the maximum handling power depends on the number of stacked FETs [5]. The shunt capacitor C_X is inserted between the two FETs in order to achieve higher isolation and low distortion characteristics.



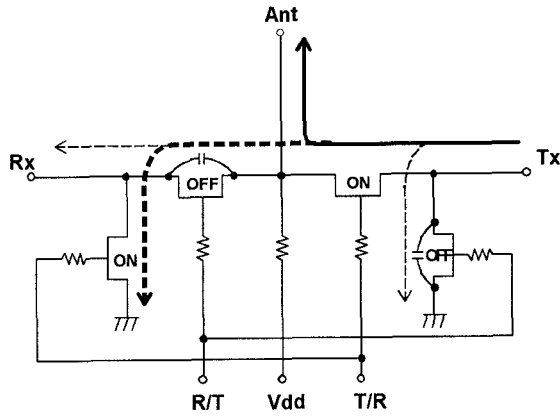


Fig. 1 (a) Circuit configuration of conventional SPDT switch.

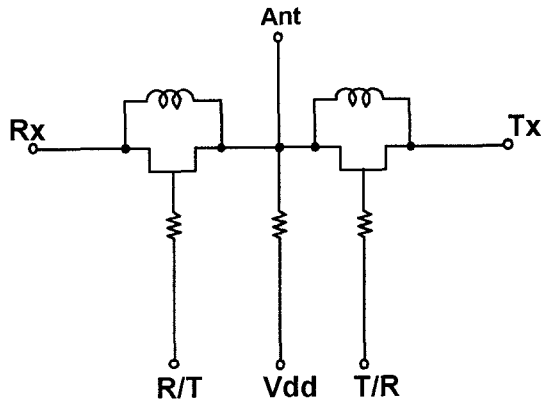


Fig. 1 (b). Circuit configuration of resonant-type SPDT switch (type A)

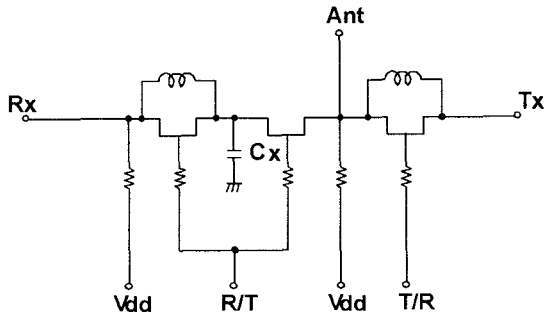
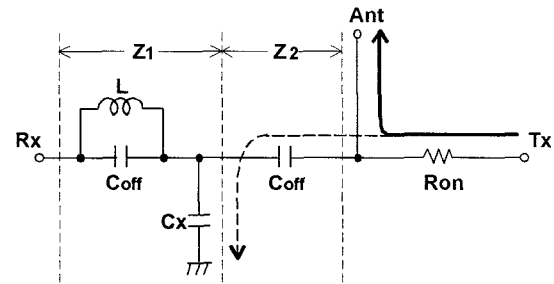


Fig.1 (c) Circuit configuration of newly-proposed resonant-type SPDT switch (type B ($C_x = 0$), type C).

The effect of C_x is explained using Fig. 2 which shows the equivalent circuit of the IC in the

transmitting mode. The on-state FETs and the off-state FETs are indicated as on-resistance (R_{on}) and off-capacitance (C_{off}), respectively. The shunt capacitor C_x lets RF signal go down to the ground-line, which causes higher isolation for the receiver input (R_x). Furthermore, we determine that the value of C_x is almost equal to that of C_{off} in order to obtain low distortion. The source-drain impedance of the FET with the inductor (Z_1) becomes equal to that of another FET (Z_2) by adding C_x , while Z_1 is quite different from Z_2 without C_x . Thus RF signal voltage swing is distributed equally to each FET by inserting C_x . This increases power-handling-capability in the transmitting mode.



$$Z_1 = \frac{1}{(j\omega_o C_{off} - \frac{1}{j\omega_o L}) + j\omega_o C_x} \approx \frac{1}{j\omega_o C_x}$$

$$Z_2 = \frac{1}{j\omega_o C_{off}}$$

if $C_x = C_{off}$ then $Z_1 \approx Z_2$

Fig. 2 Equivalent circuit of proposed SPDT switch (type C) in transmitting mode. This shows the effect of the shunt capacitor (C_x) on isolation and distortion characteristics.

FABRICATION

Fig. 3 shows a cross-sectional view of a W_N/W -gate Buried P-layer MESFET. It has a $0.6 \mu\text{m}$ self-aligned W_N/W gate with $0.3 \mu\text{m}$ -offset both at source and drain sides so that low R_{on} and high breakdown voltage can be achieved. A thin n-channel layer was formed by Si ion implantation at 45 keV and a buried p-layer was formed by Mg ion implantation. From the measured S-parameter data of MESFETs, the R_{on} was calculated to be 3.3 ohms/mm . The threshold voltage was -1.4 V and the obtained breakdown voltage was more than 6 V , which is useful to handle high-power RF signal.

Fig. 4 shows a microphotograph of the switch IC of which size is 1.15 mm x 1.05 mm. There are 50 μm -wide ground lines around the inductors, which avoid the interference among inductors and RF signal lines. The gate width of all FETs is 1 mm and the value of capacitor C_X was as low as 400 fF. Spiral inductors were electroplated to decrease the parasitic resistance.

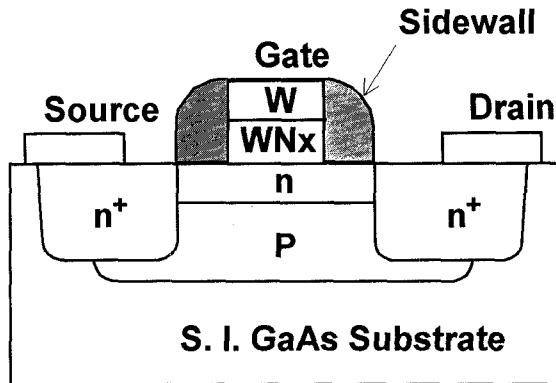


Fig. 3. Cross sectional view of 0.6 μm WN/W-gate BP-MESFET with 0.3 μm - offset for source/drain sides.

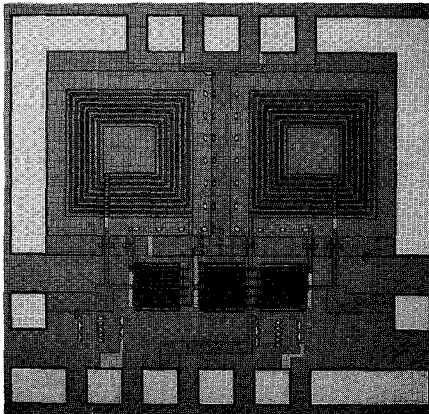


Fig. 4. Microphotograph of SPDT switch IC (type C).

PERFORMANCE

Three types of switches are compared to examine the effect of the stacked FETs and the shunt capacitor C_X inserted at the receiver side. Compared switches are type A, the resonant-type switch IC composed of single FET at the receiver side (Fig. 1(b)); type B, the resonant-type switch IC composed of stacked FETs without C_X (Fig. 1(c), $C_X = 0$); and type C, the resonant-type switch IC composed of stacked FETs with C_X which is equal to C_{off} (Fig. 1(c), $C_X = C_{\text{off}}$). Fig. 5 (a) and (b) show the measured frequency characteristics of the insertion loss and the isolation. Type C achieved the insertion loss of 0.55 dB and the isolation of 35.8 dB at 1.9 GHz. The isolation was about 8 dB lower than that of type B ($C_X = 0$), which indicated the effectiveness of an additional capacitor C_X .

The measured isolation had the minimum value at 2.1 GHz, which was slightly different from the designed value. At that resonant frequency, the isolation of type A, type B and type C were as low as 35.5 dB, 41.2 dB and 46.1 dB, respectively. For the measurements of the high order distortion and the adjacent channel leakage power, a $\pi/4$ -shifted QPSK modulated signal in the 1.9 GHz band was applied as an RF input, which is used in Japanese PHS. Fig. 6 shows the second order distortion characteristics of the switch ICs. Type C reached -54.3 dBc at 19 dBm output power, which was about 22 dB and 10 dB lower than that of type A and type B, respectively. It showed obvious difference of second order distortion between type C and others. Further the second order distortion less than -45 dBc was attained even at 21 dBm output power. Fig. 7 shows the adjacent channel leakage power. In case of type C, obtained adjacent channel leakage power at 600 kHz apart from 1.9 GHz achieved -66.0 dBc. These distortion characteristics of type C were enough for PHS applications.

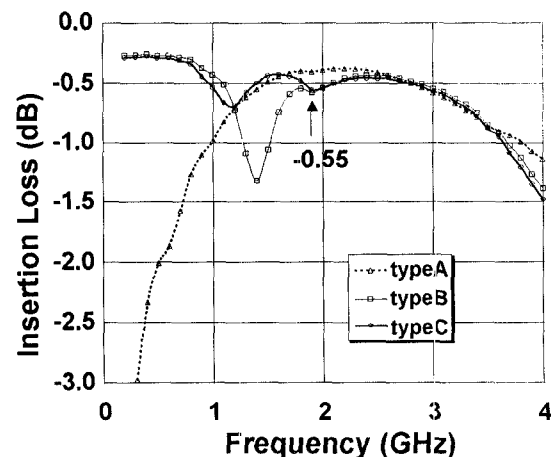


Fig. 5(a). Insertion loss characteristics of switch ICs.

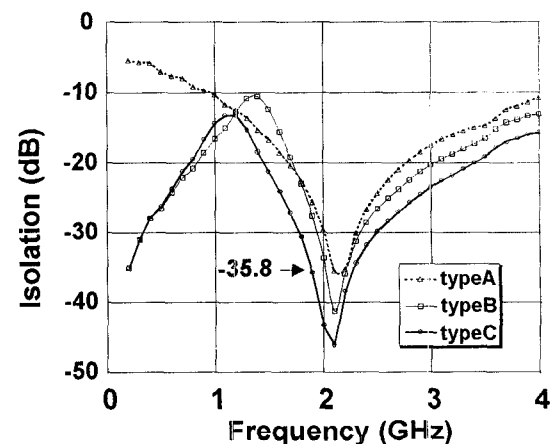


Fig. 5(b). Isolation characteristics of switch ICs.

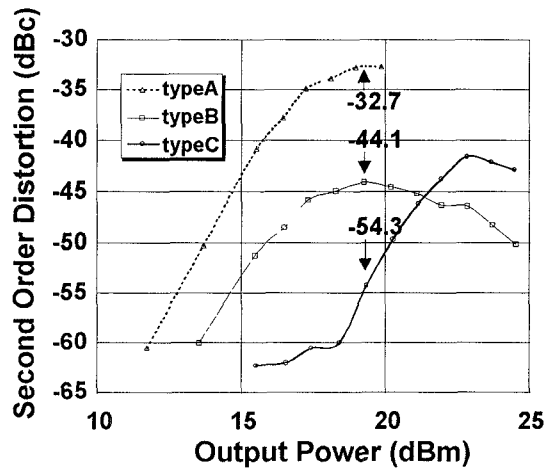


Fig.6 Second order distortion characteristics of switch ICs

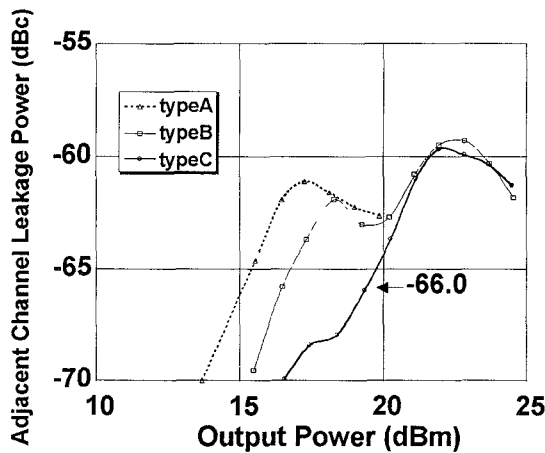


Fig. 7 Adjacent channel leakage power at 600 kHz apart from 1.9 GHz of switch ICs.

CONCLUSION

We have proposed new resonant-type GaAs switch IC and the predominant characteristics of the proposed switch IC was examined by comparing with two other resonant-type switch ICs. The proposed resonant-type switch IC which is composed of stacked FETs and an additional shunt capacitor at the receiver side showed low insertion loss of 0.55 dB, high isolation of 35.8 dB at 1.9 GHz, low second order distortion of -54.3 dBc, and low adjacent channel leakage power of -66 dBc at 19 dBm output power, with the attribution of high performance FETs which have low on-resistance and high breakdown voltage.

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